The processing challenges in making network-centric warfare a reality

By Neil Harold

With military applications demanding greater processing capability under tightening size, weight and power constraints, many developers are assessing the potential of alternative processing technologies to deliver the next step improvement in performance. Field Programmable Gate Arrays (FPGAs) and the Cell BE Processor are garnering a lot of interest, but there remain challenges to making full use of the potential of these technologies. What are the challenges to integrating these technologies into military embedded systems? And just how much performance benefit can developers expect when mapping real world applications to these architectures?

The world of processing technology is changing. Relying on Moore's law for performance improvements is no longer a guaranteed path to success, and device vendors are now considering a variety of approaches aimed at continuing the upward performance trend for next generation processing applications. This article looks at two of the highest profile technologies looking to obviate the limitations of traditional processing architectures – FPGAs and the Cell BE processor from IBM.

Nowhere is the demand for processing capability more acute than in military applications, where recent radical changes in the type of battle being fought have led to an emphasis on persistent surveillance, placing pressure on military technologies to deliver capabilities required for network-centric warfare. As doing "more with less" becomes an increasingly important strategy in military applications, developers are looking to alternative processing technologies to deliver the performance required within the size, weight, and power constraints of the wider system.

As two of the technologies garnering significant interest from military developers, FPGAs and the Cell Processor both offer a step improvement in performance capability compared with traditional processing architectures, but what are the challenges to these technologies really establishing themselves in the Defense market?

The importance of acceptance

In many ways, FPGAs can be considered the archetypal disruptive technology – highly powerful but difficult to master. Gradually however, they have achieved acceptance particularly among those who needed them most – developers of embedded military applications. This acceptance is due in no small part to the various advancements in FPGA technology in recent years, both at a device level and in the wider ecosystem. The advent of multi-million gate devices, embedded microprocessors, dedicated signal-processing units and high-speed serial links has made FPGAs increasingly competitive in both high and low-end embedded applications. Critically, these features have helped invoke a realization that FPGAs can perform floating point arithmetic – the latest Virtex-4 family from Xilinx offers a peak performance of 100GFLOPs.

Significantly for the Defense industry, there is now a wide selection of COTS vendors offering FPGA technologies on hardware platforms across a variety of forms and architectures, ranging from the FPGA-centric to the coprocessing approach. The last 2 years has also seen a marked change in the FPGA community with initiatives such as OpenFPGA (www.openfpga.org) demonstrating the type of collaborative approach that will deliver longevity to the COTS FPGA market and ultimately deliver the benefits of choice to the end users.

At a device level the Cell Processor, released by IBM in 2005, offers the type of processing performance that, much like FPGAs, makes for a compelling proposition. With a peak performance of 200GFLOPs it has huge potential for the type of real-time data intensive applications so common to the military. But achieving formal acceptance in the Defense world is a long-term play, as the FPGA community knows only too well.

With acceptance of the Cell processor in mind, the single biggest concern for military users is likely to be the fact that only one COTS vendor currently offers Cell-based platforms. This gives rise to sole source concerns, with many military programs looking for the reassurance of being able to procure similar products from other vendors. Acceptance also stems from a confidence in the longevity of a technology, which again puts a question mark against the Cell. As a new device, the Cell has no historical demonstration of technology updates while as a reference point Xilinx recently announced its 5th generation of the Virtex family of FPGAs. There is also uncertainty over the long-term future of the Cell. As the processing engine in Sony's flagship Playstation-3 gaming platform (see Figure 1), short-term volumes are virtually guaranteed. But the gaming industry is notoriously fickle and it's not clear at this stage whether the Cell will be updated for inclusion in the "Playstation-4" or whether another new technology will take its place.

Figure 1

SWAP

As mentioned at the outset of this article, military developers are under strict constraints when putting together embedded processing systems. Size and weight of both FPGA and Cell-based platforms will be a significant improvement on existing architectures, due to the reduction in overall quantity of processors required.

Power consumption has been a key factor in FPGAs gaining traction in military applications. Although the power rating of any device varies significantly depending on the application and clock speed it is running at, a range of 15-20W is a good estimate of the maximum power consumed by any member of the Virtex-4 family from Xilinx. Power consumption information for the Cell processor is hard to find, but estimates suggest that 70-80W can be expected. The difference between FPGAs and the Cell processor is mainly down to the 3.2 GHz clock frequency of the Cell, compared with the much lower 300-500 MHz rating of the FPGA.

Design challenges

No matter how compelling any processing technology is, for it to be successful it must provide a toolset and design flow that permits creation of complex applications.

Historically, this has been an area of significant challenge for FPGAs, where specialist skills and detailed architectural knowledge are deemed to be prerequisites for implementing high performance applications. The "blank" architecture of FPGAs is what simultaneously makes them hugely powerful and very difficult to program. Although there has been considerable progress in the development of high-level tools for FPGAs, with support for languages/tools such as C, MATLAB and Simulink, there remains a significant gap to be bridged before FPGAs can be programmed by users with no prior knowledge of the architecture. Work in this area would benefit considerably from greater collaboration amongst the tool and device vendors to build more cross-compatibility than is currently available, both at a card and device level.

The Cell processor is similar in the sense that the parallel architecture of the device can deliver huge performance benefits while presenting a sizeable programming challenge. The processing engine of the Cell is based on 8 Synergistic Processing Elements (SPEs), along with a Power Processor Element (PPE) for management purposes, all interconnected by a high-speed Element Interconnect Bus (EIB). Each SPE contains a Processing Unit (SPU) capable of integer and floating point arithmetic, along with a local 256 KB store and a 128x128-bit register set. From a programming perspective, the key aspect of this architecture is its complexity. Programming one of these SPUs is not an insignificant task, but mapping an application across all eight SPEs – which will be necessary to gain the type of performance available from the Cell – will require detailed planning and understanding of the target architecture both of which will add significantly to development timescales. Furthermore, the ecosystem that has started to emerge in the FPGA community will take time to form for the Cell processor and may well be stifled by the lack of a wider COTS support base (see Table 1).

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Examples of Development Tools

Design Language	Tool	Vendor
HDLs	Active-HDL	Aldec
	Leonardo Spectrum	Mentor Graphics
	Synplify	Synplicity
	XST	Xilinx
C/C++	DIME-C	Nallatech
	Handel-C	Celoxica
	Impulse-C	
	Mitrion-C	Mitrionics
Simulink	System Generator	Xilinx
MATLAB	AccelDSP	Xilinx

Table 1

Device	Fab process	Peak Performance	Peak Clock Frequency	Max Logic Cells	Max Memory	LUT Type	Power Consumption
Virtex-5	65 nm	172 GFLOPs[1]	550 MHz	331,775	1.3 MB	6-input	35-40% power reduction in Virtex-5
Virtex-4	90 nm	110 GFLOPs[2]	500 MHz	200,448	1.24 MB	4-input	

Notes

1: Peak performance achieved using V5-LX330 and 400MHz clock frequency

2: Peak performance achieved using V4-LX200 and 350MHz clock frequency

Table 2

Portability and technology upgrades

Another factor that developers will have in mind when considering these technologies is how they plan for technology upgrades. Portability has been underestimated as a success factor in the microprocessor world, often taken for granted by developers looking to port existing applications onto the latest technology. Given that processing technology can evolve 5-10 times during the lifecycle of a standard military program, it is clear that military developers have a keen interest in being able to port from one release of a technology to the next.

FPGAs deliver a certain class of portability between different evolutions of device families and even between vendors. Moving from one version of a device family to the next – say Virtex-4 to Virtex-5 – is a very straightforward task (see Table 2). Clearly, where a design uses a piece of fixed silicon such as the embedded DSP Blocks in the Virtex family, to achieve comparable or better performance it is necessary that the next generation device has support for this feature. The silicon vendors have historically been very good at this type of backwards compatibility. Even porting from a Xilinx Virtex-4 device to a Stratix-II from Altera is a relatively simple task, with HDL acting as a kind of middleware that is agnostic of the hardware architecture being targeted.

The novel architecture of the Cell BE will make porting applications from traditional microprocessors a challenging proposition. Although the language may stay the same, the parallel architecture, as highlighted earlier, will demand reworked code in order to even get an application functioning correctly, never mind achieving an increase in performance. Portability is also hugely constrained by the fact that the Cell is a one-off device, with no equivalent alternative technology available from other vendors. Future portability is also an unknown quantity given that the long-term roadmap for the Cell is still unclear and potential users can't even derive comfort from having millions of devices across multiple generations deployed and in use.

Conclusion

As processing technologies continue to change, there is no doubt that the Cell processor and FPGAs will compete, particularly in military applications. The decision over which option to take will be influenced by a range of dynamics, but it could yet be that a rounded ecosystem will prove to be a decisive factor in convincing users to adopt a particular technology. On this basis, it appears that even the Cell with its mighty backers has some way to go before it establishes itself as a viable alternative to the current "alternative" processing technologies.

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