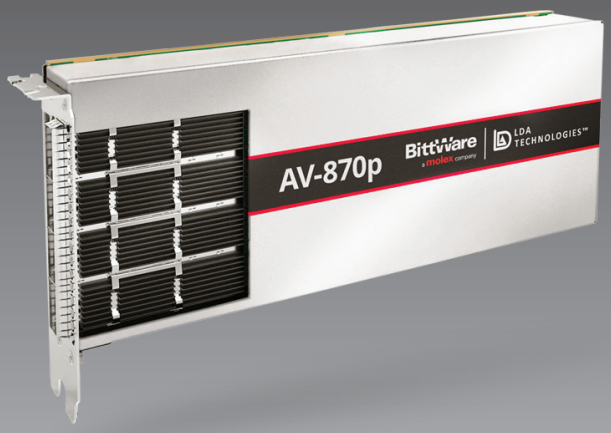
BittWare a molex company

AV-870p
PCIe Adaptive SoC Card

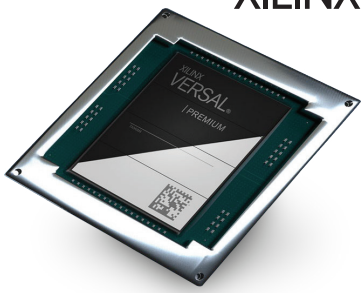


LDA

Versal™ Premium Adaptive SoC Card
400G and PCIe Gen5

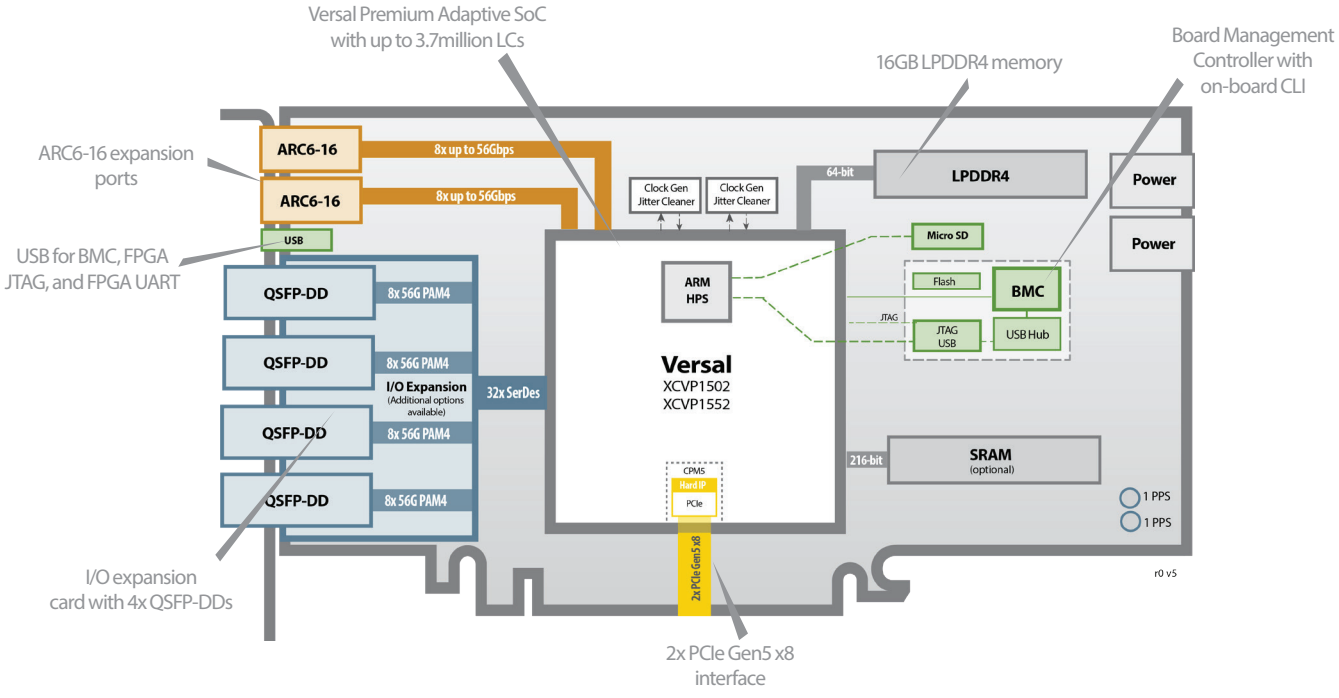
Brought to market in partnership with LDA Technologies, the AV-870p is a PCIe Gen5 accelerator card designed to deliver extreme performance for data center and edge compute workloads. Featuring AMD Xilinx®'s Versal Premium Adaptive SoC, the AV-870p is a deployment-ready full height, ¾ length PCIe accelerator compatible with high-performance servers. The card features QSFP-DDs for up to 3x 400G, 2x PCIe Gen5 x8, and a sophisticated Board Management Controller (BMC) for advanced system monitoring and control.

AMD XILINX



key features

- Up to **3x 400G**
- **2x PCIe Gen5** x8
- **Versal Premium** with up to **3.7M Logic Cells**

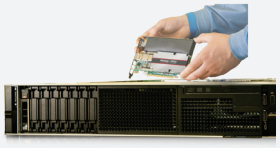


Additional Services

Take advantage of BittWare's range of design, integration, and support options

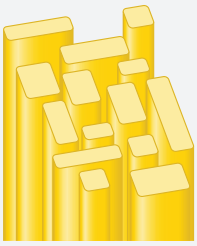
Customization

Additional specification options or accessory boards to meet your exact needs.



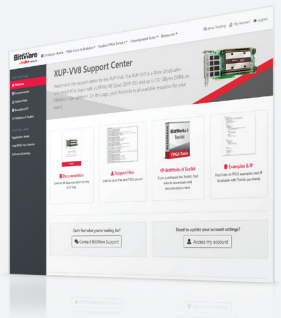
Server Integration

Available pre-integrated in our TeraBox servers in a range of configurations.



IP and Solutions

Our portfolio of IP and solutions reduce risk for development and deployment.



Service and Support

BittWare Developer Site provides online documentation and issue tracking.

Board Specifications

Adaptive SoC	• Versal Premium
	  • VP1502/ VP1552
	  • Core speed grade - 2
	• Contact BittWare for other FPGA options

On-board Flash	• Flash memory for booting FPGA

External memory	• 2x 8GB LPDDR4 chips (16GB total) @ 4266MHz (64 bits) accessible to ARM and FPGA logic via NOC
	• 432 MB of ultra-low-latency GSI SRAMs (optional)
	  • 12x 18-bit chips
	  • 216-bit total bus width

Host interface	• 2x PCIe x8 Gen5 interfaces direct to FPGA, connected to PCIe Hard IP

I/O Expansion	• I/O expansion site connected to FPGA via 32x SerDes channels:
	  • VP1502: 32 GTM
	  • VP1552: 16 GTYP and 16 GTM
	• 2x ARC6-16 connectors connected to FPGA via 8x SerDes channels each (16x total)
	  • VP1502: 16x GTM 56Gbps channels
	  • VP1552: 16x GTYP 32Gbps channels

QSFP-DD Module	• Default I/O module features 4x QSFP-DD cages on front panel supporting 56G PAM4 (uses 32x SerDes) • Additional custom modules available. Contact BittWare.
Clocking	• 2x Jitter cleaners for network recovered clocking • 2x 1PPS (in-board)
USB	• USB access to BMC, USB-JTAG, USB-UART
Board Management Controller	• Onboard CLI • Python, C++ API (contact BittWare) • 200 Mbps parallel port connected to the FPGA fabric and the NO • USB SD Card Reader for simple OS images transfer to ARM processors • Fast FPGA Boot Flash programming • Temperature, voltage, current monitoring • SNMP agent for centralized management • Dedicated preprogrammed array of 32 MAC addresses • I/O port monitoring full QSFP, SFP, QSFP-DD access and programming through CLI and API • CLI-based clock selection supporting custom clock configurations
Cooling	• Standard: dual-width passive heatsink
Electrical	• On-board power derived from 12V PCIe slot and 2x AUX connectors • Power dissipation is application dependent
Environmental	• Operating temperature 5°C to 35°C
Form factor	• ¾-length, standard-height PCIe dual-width board • 10 x 4.37 inches (254 x 111.15 mm)

Development Tools

Application development	Supported design flows -Vivado Design Suite (HDL, Verilog, VHDL, etc.)

To learn more, visit **www.BittWare.com**

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LDA TECHNOLOGIES™

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